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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,489	04/12/2004	Hongjian Gan	JCLA12709	4944
23900	7590	09/05/2007		
J C PATENTS, INC. 4 VENTURE, SUITE 250 IRVINE, CA 92618			EXAMINER RUTLAND WALLIS, MICHAEL	
			ART UNIT 2836	PAPER NUMBER
			MAIL DATE 09/05/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/823,489

Applicant(s)

GAN ET AL.

Examiner

Michael Rutland-Wallis

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 July 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/12/2007 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 15, 18 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of Bourdillon (U.S. Pat. No. 6,552,917)

With respect to claims 1, 15 and 18 AAPA teaches a power supply with multiple outputs (Fig. 1), comprising: a front-end converter (item 1) with a current mode output; a

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first buck converter (items 2) and a second buck converter (items 3), both of which cascade from a first output capacitor (item Cf) of the front-end converter (item 1). AAPA does not teach a time delay synchronous control circuit, for controlling a delay time between the time the front-end converter begins to have a pulse current to the first output capacitor and the time the first buck converter and the second buck converter being turned on is adjusted. Bourdillon teaches a controller (connection of fast loop controller and slow loop controller 320) for controlling a delay time (T1-T6) between the time the front-end converter begins to have a pulse (from T2 to T6 discharging time) and the time the first buck converter and the second buck converter being turned on (discharge time) is adjusted. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA to include circuitry to control the switching of the main switch and buck switches in order to allow soft switching and voltage regulation.

With respect to claim 22 and 24 AAPA teaches A power supply with multiple output (Fig. 1), comprising a converter (item 1), a output capacitor (item Cf); and a buck converter (items 2 and 3), directly cascading the output capacitor (item Cf) of the converter (1), wherein the buck converter is controlled by a buck switch (items S1 and S2), the buck switch begins to turn on at the time when the converter has a pulse current to the output capacitor and lure off at the time before the time when the main switch turns on. AAPA does not teach a rectifier or the buck switch begins to turn on at the time when the converter has a pulse current to the output capacitor and lure off at the time before the time when the main switch turns on. Bourdillon teaches a buck

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switch (such as S1) is turned at the time (beginning T2 see Fig. 4a) when the converter has a pulse current (i.e. the pulse discharge phase T2-T6) and turn off (see switching off of buck switches in Fig. 4a) at the time before the time when the main switch turns on. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA to use a diode rectifier or to control the buck switch as claimed to allow for the clean soft switching of output voltages.

With respect to claim 23 Bourdillon teaches the converter is a flyback converter (see abstract).

Claims 2-14, 16-17 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of Bourdillon (U.S. Pat. No. 6,552,917) in further view of Huang et al. (U.S. Pat. No. 6,344,979)

With respect to claim 2 AAPA as modified by Bourdillon do not teach the converter is a LLC-SRC as described, Huang teaches such a converter. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize such a converter in order to power conversion efficiency and switching.

With respect to claims 3 and 4 AAPA as modified by Bourdillon do not teach is silent on the internal circuitry of the front-end converter. Huang teaches the front-end converter comprising: a bridge circuit including (bridge rectifier) a pair of power switches (diodes), the bridge circuit being coupled to an input voltage; a resonant tank (formed with capacitor and inductor). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the use of a additional circuitry of a tank circuit

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and control as such circuitry in order to output a clear power signal as such circuitry is typical in such converters.

With respect to claim 5 and 6 Huang teaches the resonant tank comprising: a series resonant capacitor (C_s), coupled to the bridge circuit (S1 and S2 or see Giannopoulos); a series resonant inductor (L_s), coupled to the series resonant capacitor; and a transformer (item 130) with a magnetizing inductor coupled to the series resonant inductor and the bridge circuit, wherein the series resonant capacitor, the series resonant inductor and the magnetizing inductor constitute two characteristic frequencies of the resonant tank.

With respect to claim 7 AAPA teaches the bridge circuit comprises a bus capacitor (Fig. 1) coupled to the input voltage.

With respect to claim 8 Huang teaches the transformer comprising a primary winding and two secondary windings connected in series in phase, for isolating the bridge circuit and the resonant tank from the rectifier.

With respect to claims 9 and 10 Huang as modified above teaches the rectifier is a full-wave rectifier comprising a first rectifier diode and a second rectifier diode connected to the output capacitor, the first and second rectifier diodes are connected through the output capacitor to an output filter (rectifier and LC circuit) to generate an output voltage of the multiple outputs of the power supply.

With respect to claims 11 and 19 Bourdillon teaches the delay time behind the time when the front-end converter begins to have the pulse (T2) output current, the first buck converter (via S1) and the second buck converter (via S2) are sequentially turned

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on and then the first buck converter is turned off after the second buck converter is turned off (see Fig. 4a).

With respect to claim 12 and 17 Bourdillon teaches buck switches (S1 and S2) of both the first and second buck converters are turned off before the pulse output current of the front-end converter reaches to zero (see dissipated returned energy T_{bound} shown in Fig. 4b-d).

With respect to claims 13 and 20 Bourdillon teaches the delay time behind the time when the front-end converter begins to have the pulse output current, the first buck converter is turned on and then the first buck converter is turned off (T2-T3), at the time (T3) the first buck converter being turned off (T3), the second buck converter is sequentially turned on (T3-T4).

With respect to claim 14, 16 and 21 Bourdillon teaches a dead conduction time interval (off time of main switch between T2 and T6) exists between every two of the output current pulses of the front-end converter, the first buck converter and the second buck converter are sequentially turned (see Fig. 4a) on and then the first buck converter is turned off before the second buck converter is turned off, an overlap existing (col. 5 lines 5-10) between the period of the first buck converter being on and the period of the second buck converter being on.

Allowable Subject Matter

The indicated allowability of claims 1-21 are withdrawn in view of the newly discovered references to cited above. Rejections based on the newly cited references are found above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Goder et al. (U.S. Pat. No. 5,617,015) teaches a similar synchronous control system as Applicant's claimed system.

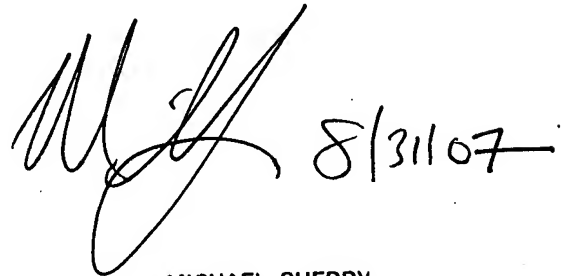
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MRW

A handwritten signature in black ink, appearing to read 'MS', followed by the date '8/31/07' written in a similar cursive style.

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800